Amendment to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. – 34. (canceled)

35. (previously presented) An NMOS transistor comprising:

a dielectric layer above a substrate;

a trench in said dielectric layer, wherein the bottom of said trench is directly above said substrate;

a gate dielectric layer in said trench, wherein a first portion of said gate dielectric layer is adjacent to a first sidewall of said trench, wherein a second portion of said gate dielectric layer is adjacent to a second sidewall of said trench, and wherein a third portion of said gate dielectric layer is on the bottom of said trench;

a gate electrode in said trench, wherein said gate electrode is directly between said first and said second portions of said gate dielectric layer, wherein said gate electrode is comprised of a central portion and a pair of outer portions, wherein said outer portions are each comprised of a sidewall region and an extension region, wherein said central portion is directly adjacent to said sidewall region and directly above said extension region of each of said outer portions, wherein the bottom surfaces of said central portion and said pair of outer portions are

directly on said third portion of said gate dielectric layer, and wherein the workfunction of said pair of outer portions is lower than the workfunction of said central portion; and

a pair of n type source/drain regions in said substrate on opposite sides of said pair of outer portions of said gate electrode.

36. (previously presented) The transistor of claim 35 wherein the workfunction of said central portion is between 3.9 to 4.3 eV.

37. (previously presented) The transistor of claim 36 wherein the workfunction of said pair of outer portions is between 1.5 to 3.8 eV.

38. (previously presented) The transistor of claim 35 wherein the workfunction of said pair of outer portions is at least 0.1 eV lower than the workfunction of said central portion.

39. (previously presented) The transistor of claim 35 wherein said pair of outer portions is formed from a material selected from the group consisting of scandium (Sc), magnesium (Mg) and Yttrium (Y).

40. (previously presented) The transistor of claim 39 wherein said central portion comprises a conductive material selected from the group consisting of poly-silicon, titanium, zirconium, hafnium, tantalum, and aluminum.

41. (canceled)

42. (previously presented) The transistor of claim 35 wherein said pair of outer portions of said gate electrode overlap said pair of n type source/drain regions.

43. (previously presented) A PMOS transistor comprising:

a dielectric layer above a substrate;

a trench in said dielectric layer, wherein the bottom of said trench is directly above said substrate;

a gate dielectric layer in said trench, wherein a first portion of said gate dielectric layer is adjacent to a first sidewall of said trench, wherein a second portion of said gate dielectric layer is adjacent to a second sidewall of said trench, and wherein a third portion of said gate dielectric layer is on the bottom of said trench;

a gate electrode in said trench, wherein said gate electrode is directly between said first and said second portions of said gate dielectric layer, wherein said gate electrode is comprised of a central portion and a pair of outer portions, wherein said outer portions are each comprised of a sidewall region and an extension region, wherein said central portion is directly adjacent to said sidewall region

and directly above said extension region of each of said outer portions, wherein the bottom surfaces of said central portion and said pair of outer portions are directly on said third portion of said gate dielectric layer, and wherein the workfunction of said pair of outer portions is higher than the workfunction of said central portion; and

a pair of p type source/drain regions in said substrate on opposite sides of said pair of outer portions of said gate electrode

44. (previously presented) The transistor of claim 43 wherein the workfunction of said central portion is between 4.9 to 5.3 eV.

45. (previously presented) The transistor of claim 44 wherein the workfunction of said pair of outer portions is between 5.4 to 6.0 eV.

46. (previously presented) The transistor of claim 43 wherein the workfunction of said pair of outer portions is at least 0.1 eV higher than the workfunction of said central portion.

47. (previously presented) The transistor of claim 43 wherein said pair of outer portions is formed from a material selected from the group consisting of poly-silicon, platinum, and ruthenium nitride (RuN).

48. (previously presented) The transistor of claim 47 wherein said central portion comprises a conductive material selected from the group consisting of ruthenium and palladium.

49. (canceled)

50. (previously presented) The transistor of claim 43 wherein said pair of outer portions of said gate electrode overlap said pair of p type source/drain regions.

51. (previously presented) The transistor of claim 35, further comprising:

a pair of n type tip extensions adjacent to said pair of n type source/drain regions, wherein said extension regions of said pair of outer portions of said gate electrode partially overlap said pair of n type tip extensions.

52. (previously presented) The transistor of claim 35, further comprising:

a pair of n type tip extensions adjacent to said pair of n type source/drain regions, wherein said extension regions of said pair of outer portions of said gate electrode are substantially in alignment with said pair of n type tip extensions.

53. (previously presented) The transistor of claim 35, further comprising:

a pair of n type tip extensions adjacent to said pair of n type source/drain regions; and

a channel region in between said pair of n type tip extensions, wherein said extension regions of said pair of outer portions of said gate electrode completely overlap said pair of n type tip extensions and partially overlap said channel region.

54. (previously presented) The transistor of claim 35 wherein said central portion of said gate electrode covers at least 50% of said third portion of said gate dielectric layer on the bottom of said trench.

55. (previously presented) The transistor of claim 54 wherein said central portion of said gate electrode covers at least 70% of said third portion of said gate dielectric layer on the bottom of said trench.

56. (previously presented) The transistor of claim 35 wherein one of the outer portions of said pair of outer portions of said gate electrode is ⌊-shaped and the other outer portion of said pair of outer portions of said gate electrode is ⌋-shaped.

57. (previously presented) The transistor of claim 43, further comprising:

a pair of p type tip extensions adjacent to said pair of p type source/drain regions, wherein said extension regions of said pair of outer portions of said gate electrode partially overlap said pair of p type tip extensions.

58. (previously presented) The transistor of claim 43, further comprising:

a pair of p type tip extensions adjacent to said pair of p type source/drain regions, wherein said extension regions of said pair of outer portions of said gate electrode are substantially in alignment with said pair of p type tip extensions.

59. (previously presented) The transistor of claim 43, further comprising:

a pair of p type tip extensions adjacent to said pair of p type source/drain regions; and

a channel region in between said pair of p type tip extensions, wherein said extension regions of said pair of outer portions of said gate electrode completely overlap said pair of p type tip extensions and partially overlap said channel region.

60. (previously presented) The transistor of claim 43 wherein said central portion of said gate electrode covers at least 50% of said third portion of said gate dielectric layer on the bottom of said trench.

61. (previously presented) The transistor of claim 60 wherein said central portion of said gate electrode covers at least 70% of said third portion of said gate dielectric layer on the bottom of said trench.

62. (previously presented) The transistor of claim 43 wherein one of the outer portions of said pair of outer portions of said gate electrode is ⌊-shaped and the other outer portion of said pair of outer portions of said gate electrode is ⌋-shaped.

63. (currently amended) A transistor comprising:

a dielectric layer above a substrate;

a trench in said dielectric layer, wherein the bottom of said trench is directly above said substrate;

a gate dielectric layer on the bottom of said trench;

a gate electrode in said trench, wherein said gate electrode is comprised of a central portion and a pair of outer portions, wherein said outer portions are each comprised of a sidewall region and an extension region, wherein said central portion is directly adjacent to said sidewall region and directly above said extension region of each of said outer portions, wherein the bottom surfaces of said central portion and said pair of outer portions of said gate electrode are directly on said gate dielectric layer on the bottom of said trench, and wherein the workfunction of said pair of outer portions is different than the workfunction of said central portion; and

a pair of source/drain regions in said substrate on opposite sides of said pair of outer portions of said gate electrode.

64. (previously presented) The transistor of claim 63 wherein the workfunction of said pair of outer portions is at least 0.1 eV different than the workfunction of said central portion.

65. (previously presented) The transistor of claim 63, further comprising:

a pair of tip extensions adjacent to said pair of source/drain regions, wherein said extension regions of said pair of outer portions of said gate electrode partially overlap said pair of tip extensions.

66. (previously presented) The transistor of claim 63, further comprising:

a pair of tip extensions adjacent to said pair of source/drain regions, wherein said extension regions of said pair of outer portions of said gate electrode are substantially in alignment with said pair of tip extensions.

67. (previously presented) The transistor of claim 63, further comprising:

a pair of tip extensions adjacent to said pair of source/drain regions; and

a channel region in between said pair of tip extensions, wherein said extension regions of said pair of outer portions of said gate electrode completely overlap said pair of tip extensions and partially overlap said channel region.

68. (previously presented) The transistor of claim 63 wherein said central portion of said gate electrode covers at least 50% of said gate dielectric layer on the bottom of said trench.

69. (previously presented) The transistor of claim 68 wherein said central portion of said gate electrode covers at least 70% of said gate dielectric layer on the bottom of said trench.

70. (previously presented) The transistor of claim 63 wherein one of the outer portions of said pair of outer portions of said gate electrode is ⌊-shaped and the other outer portion of said pair of outer portions of said gate electrode is ⌋-shaped.